IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Darin J. Douma	
Application No.:	10/678,685	Art Unit 2611
Filed:	October 03, 2003	
Conf. No.:	9973	
For:	CIRCUIT FOR CONVERTING A TRANSPONDER CONTROLLER CHIP OUTPUT INTO AN APPROPRIATE INPUT SIGNAL FOR A HOST DEVICE	
Examiner:	Linda Wong	
Customer No.:	22913	
Attorney Docket No.:	15436.250.24.1	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Final Office action mailed August 12, 2010 (the "Office Action"), Applicants respectfully request a panel review of the final rejection under 35 U.S.C. § 103(a) discussed in the remarks below. No amendments are being filed with this Request. This Request is being filed concurrently with a Notice of Appeal.

Reconsideration of the application by a panel of examiners is respectfully requested in view of the following remarks. Please note that the following remarks are not intended to be an exhaustive enumeration of the distinctions between any cited references and the claimed invention. Rather, the distinctions identified and discussed below are presented solely by way of example to illustrate some of the clear errors in the rejection.

REMARKS

The Office Action rejects the claims under 35 U.S.C §103(a) as being unpatentable over various combinations of *Lutz* (U.S. Patent No. 4,276,548) with other references. Applicants submit, however, that certain mischaracterizations of *Lutz* discussed below constitute clear errors and, therefore, withdrawal of the rejection is respectfully requested.

A. Independent Claim 14

Claim 14 recites a method comprising, among other things:

> receiving a synchronization signal from a phase locked loop…;
>
> obtaining an average of the synchronization signal over a period of time; [and]
>
> comparing the average of the synchronization signal with a reference signal to determine whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency.

(Emphasis added.) For example, as discussed in Applicants' specification, circuitry depicted in Figure 4 of Applicants' specification (copied below) uses a capacitor (76) to obtain an average of a synchronization signal (V_{PLL}) over a period of time and then uses a comparator (70) to compare the average with a references signal (V_{REF}). *See* Applicants' specification at ¶¶ 39 and 40.

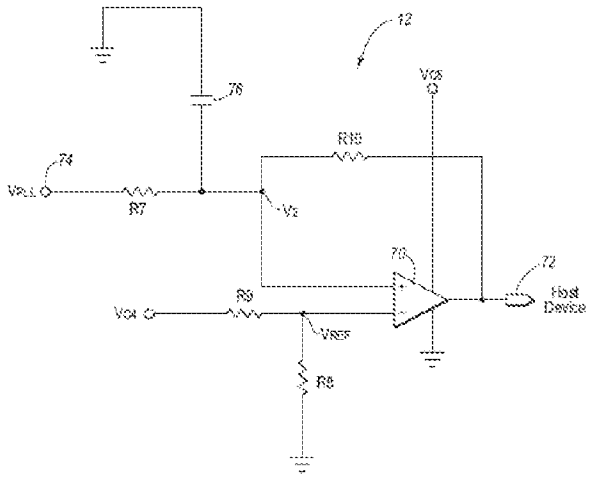

Fig. 4

In contrast, the cited art, whether considered individually or in combination, fails to teach or suggest the foregoing limitations.

The Examiner concedes *APA* fails to disclose the foregoing limitations but asserts that *Lutz* describes a timer 16 that receives a PLL development signal from PLL 14 (on line 44) and "measures over a period of time whether the signal on line 44 is stable." *See Office Action* at 15 and 16. However, measuring whether a signal on a line is stable over a period of time does not constitute "obtaining an average" of the signal over the period of time, as claimed. For example, if the signal on line 44 becomes unstable for a brief moment during the measuring period of time, *Lutz's* timer 16 will determine the signal is unstable and begin measuring anew, whereas an average of the signal over the same period of time will indicate otherwise.

In light of the foregoing, the Examiner's rejection claim 14 is based on a mischaracterization of *Lutz* and should be withdrawn.

B. Independent Claim 19

Claim 19 recites, among other things, "a timing circuit adapted to measure a period of time that the synchronization signal is asserted using at least a capacitor arranged to discharge when the synchronization signal is asserted and to charge when the synchronization signal is not asserted." (Emphases added.) In contrast, the prior art references, whether considered individually or in combination, fail to teach or suggest the foregoing limitation.

For example, the Examiner first identifies a capacitor 318 of Lutz as corresponding to the claimed capacitor. *See Office Action* at 11 and 12 ("Lutz discloses a timing circuit adapted to measure a period of time…using at least a capacitor…(…Col. 8, lines 19-22 discloses 'A predetermined time after synchronization is achieved, the potential developed across capacitor 318 will rise….')."") However, in the response to arguments section, the Examiner concedes that capacitor 318 "charges when the PLL is in a state of synchronization." *See Office Action* at 3. Therefore, the Examiner appears to concede capacitor 318 does not correspond to the claimed "capacitor arranged to discharge when the synchronization signal is asserted." In fact, according to *Lutz*, capacitor 318 begins charging when the lock signal on line 44 (identified as the claimed "synchronization signal") becomes stable. *See Lutz* at col. 3, lines 56-59 and col. 8, lines 19-22

(A predetermined time after synchronization is achieved, the potential developed across 318 will rise….")

The Examiner also appears to identify a capacitor 360 in *Lutz* as corresponding to the claimed "capacitor." However, capacitor 360 is not used to time how long the lock signal on line 44 is asserted. Instead, capacitor 360 is part of a timer 18 that governs an amount of time that a reading of the stabilized PLL's frequency is performed. *See Lutz* at col. 4, lines 62-68 and col. 5, lines 1-3, and Figure 3B.

Moreover, the Examiner's assertion that capacitor 360 will "charge" when the PLL is "not in a state of synchronization" (*See Office Action* at 4) is incorrect. Like capacitor 318, capacitor 360 charges when measuring the period of time to read the stabilized PLL's frequency. *See Lutz* at col. 9, lines 14-17. More specifically, capacitor 360 charges between times 120 and 122 in the timing diagram of *Lutz's* Figure 2 (copied below with annotations). As shown in the timing diagram, the PLL is in a state of synchronization during this time because the lock signal on line 44 is stable. Therefore, contrary to the Examiner's assertion, capacitor 360 charges when the PLL is in a state of synchronization.

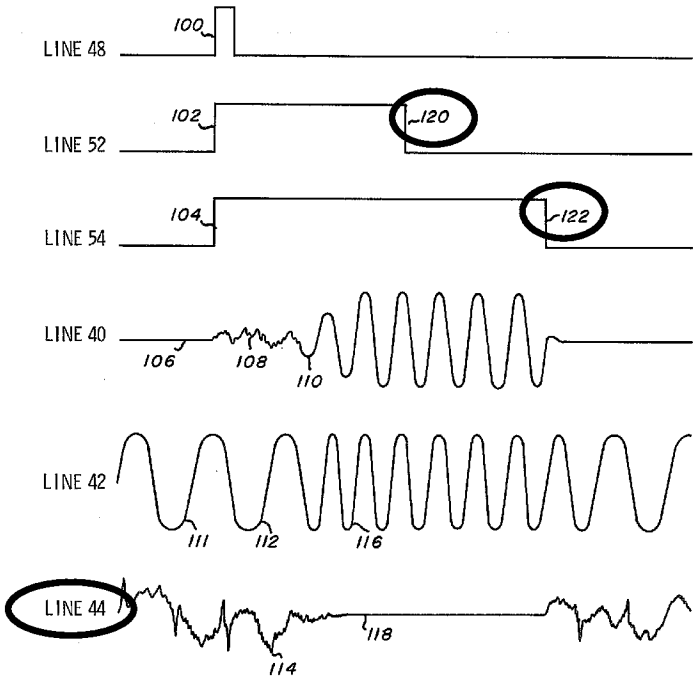

Fig_2

In light of the foregoing, the Examiner's rejection claim 19 is based on mischaracterizations of *Lutz* and should be withdrawn.

Charge Authorization

The Commissioner is hereby authorized to charge payment of any of the following fees that may be applicable to this communication, or credit any overpayment, to Deposit Account No. 23-3178: (1) any filing fees required under 37 CFR § 1.16; (2) any patent application and reexamination processing fees under 37 CFR § 1.17; and/or (3) any post issuance fees under 37 CFR § 1.20. In addition, if any additional extension of time is required, which has not otherwise been requested, please consider this a petition therefor and charge any additional fees that may be required to Deposit Account No. 23-3178.

Dated this 13th day of December 2010.

Respectfully submitted,

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